STP4407

P Channel Enhancement Mode MOSFET

- 10A

DESCRIPTION

The STP4407 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density, DMOS J0ь

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STP4407

ELECTRICAL CHARACTERISTICS (Ta = 25℃ Unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,ID=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},ID=-250uA	-1.0		-2.5	V
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V			-1	uA
	T_J=55℃	V_{DS}=-30V,V_{GS}=0V			-5	
Drain-source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-10A V_{GS}=-4.5V,I_D=-6.0A		15 24	20 32	mΩ
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-10A		26		S
Diode Forward Voltage	V_{SD}	I_S=-1				V

2 444.32 Tc 144 -1.44 ref410.64 606.56 ( )]TJ330.490.0487

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TYPICAL CHARACTERICTICS

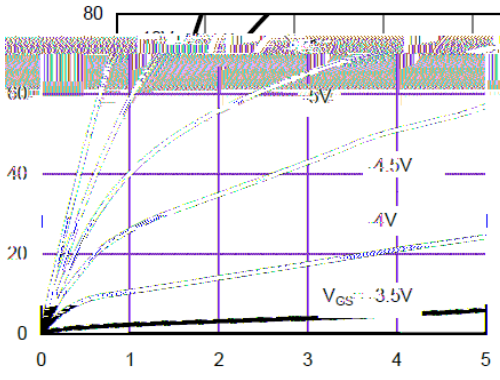


Figure 1: On-Region Characteristics

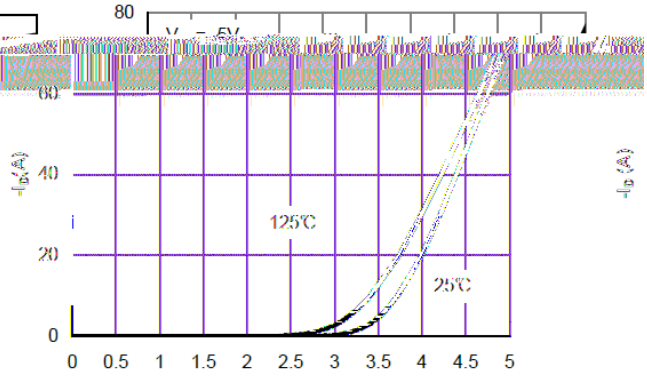


Figure 2: Transfer Characteristics

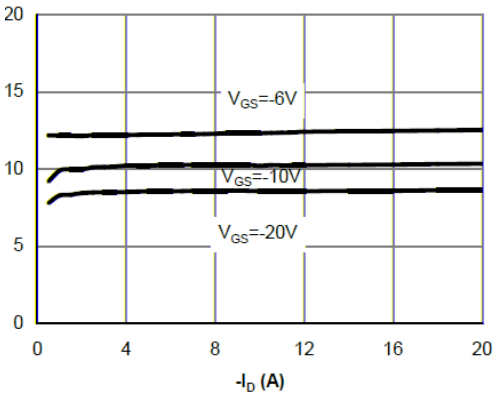


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

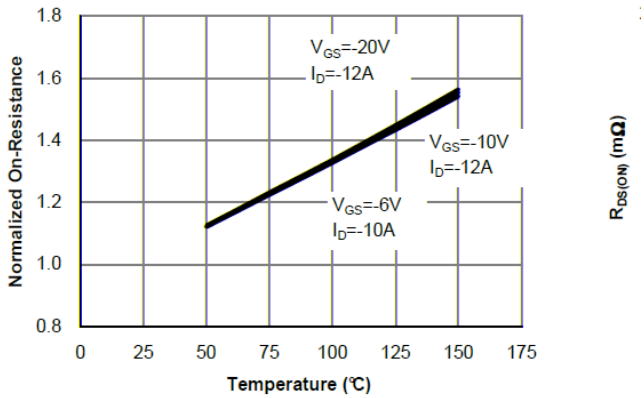
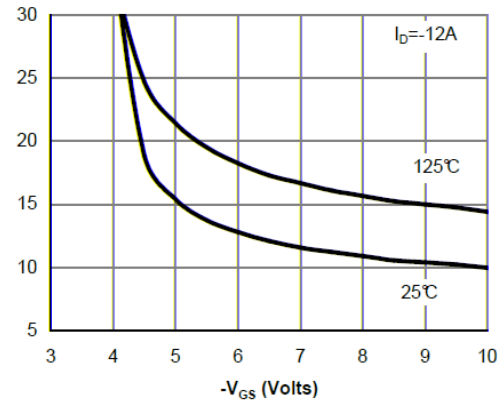
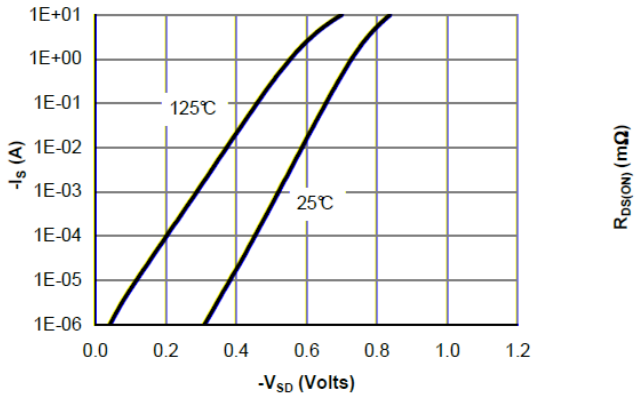


Figure 4: On-Resistance vs. Junction Temperature





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TYPICAL CHARACTERICTICS

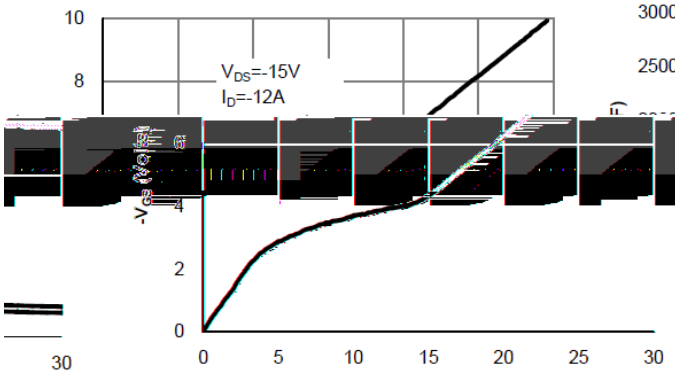

Figure 7: Gate-Charge Characteristics

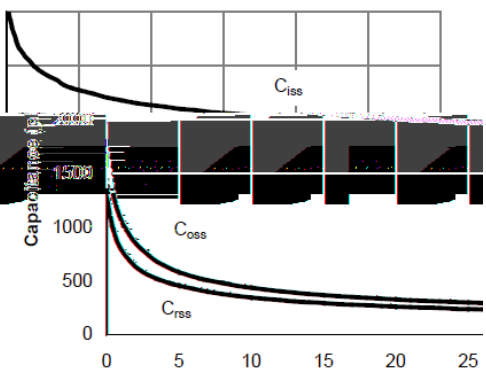

Figure 8: Capacitance Characteristics

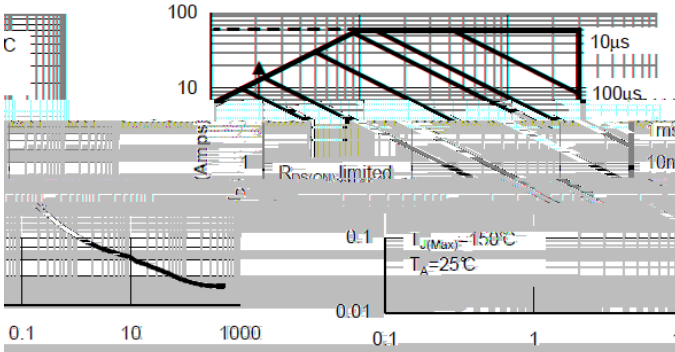

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

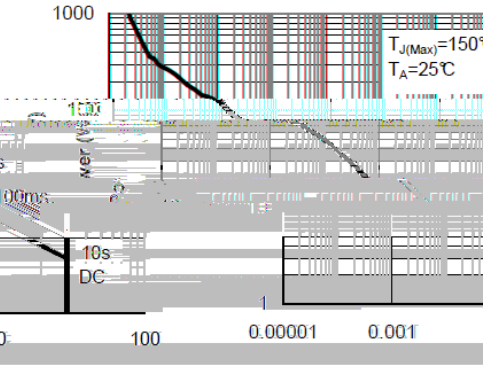

Figure 10: Single Puls to-Ambi

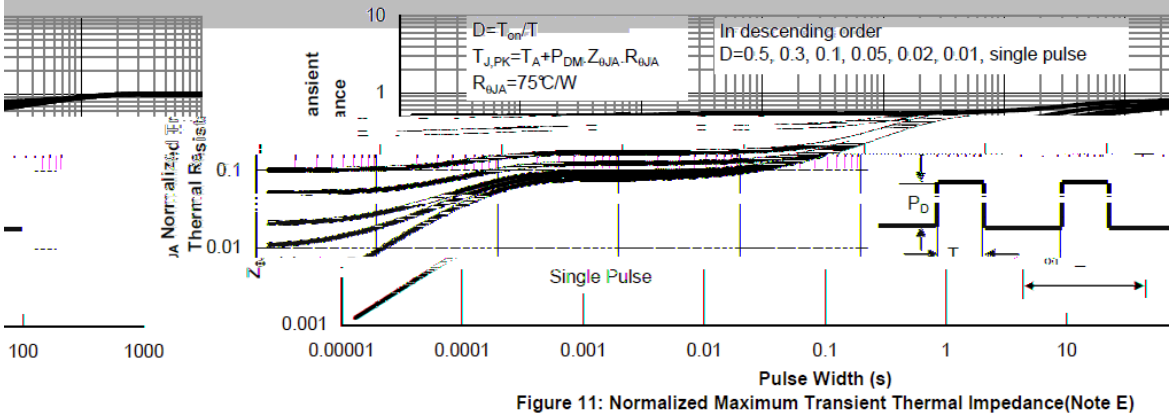

Figure 11: Normalized Maximum Transient Thermal Impedance(Note E)

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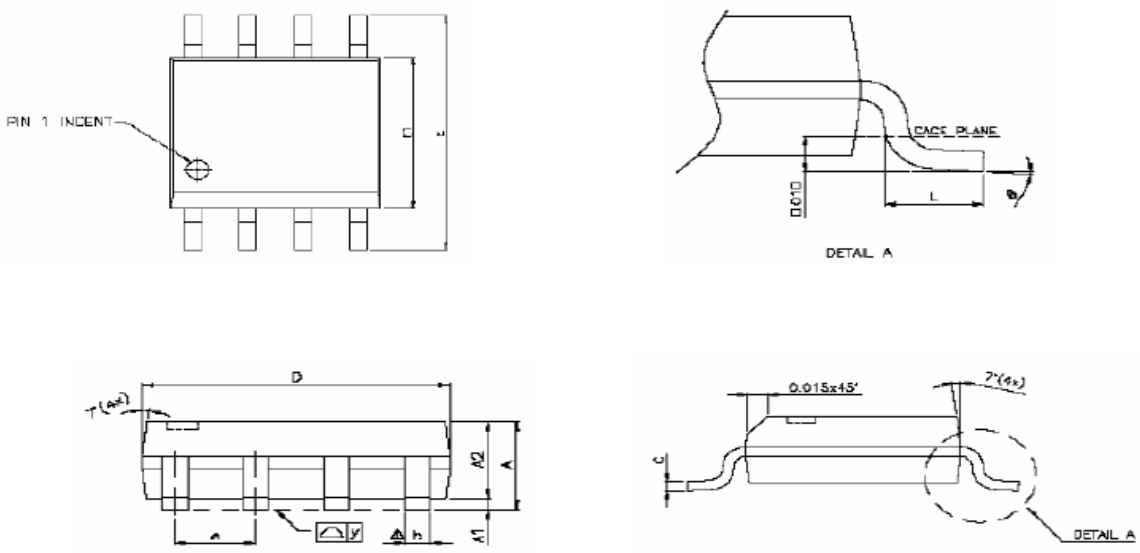
PACKAGE OUTLINE SOP-8P



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10		0.25	0.004		0.010
A2	1.45			0.057		
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.19	0.20	0.25	0.008	0.008	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
L	0.38	0.71	1.27	0.015	0.028	0.050
y			0.076			0.003
θ	0°	4°	8°	0°		8°

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